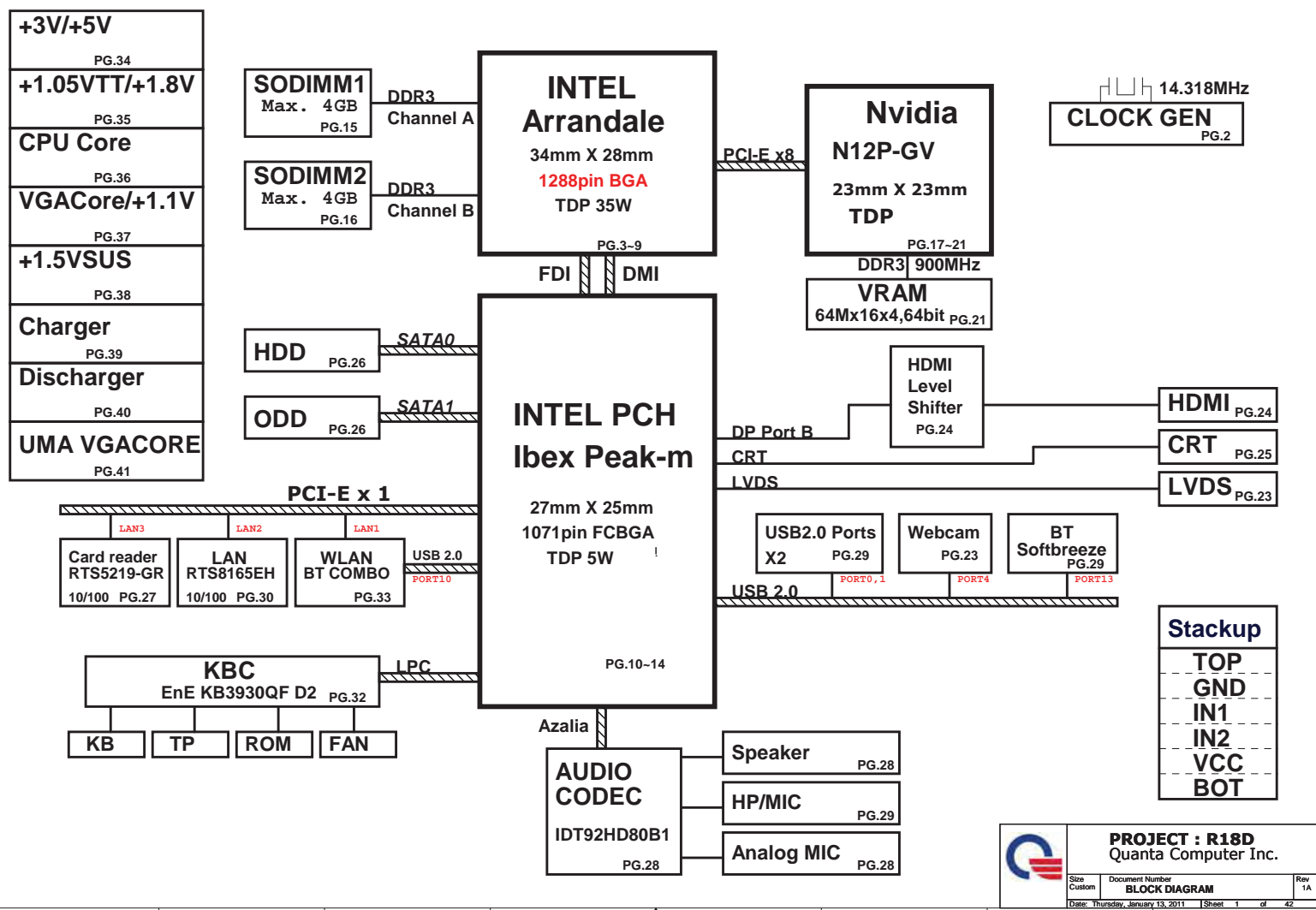
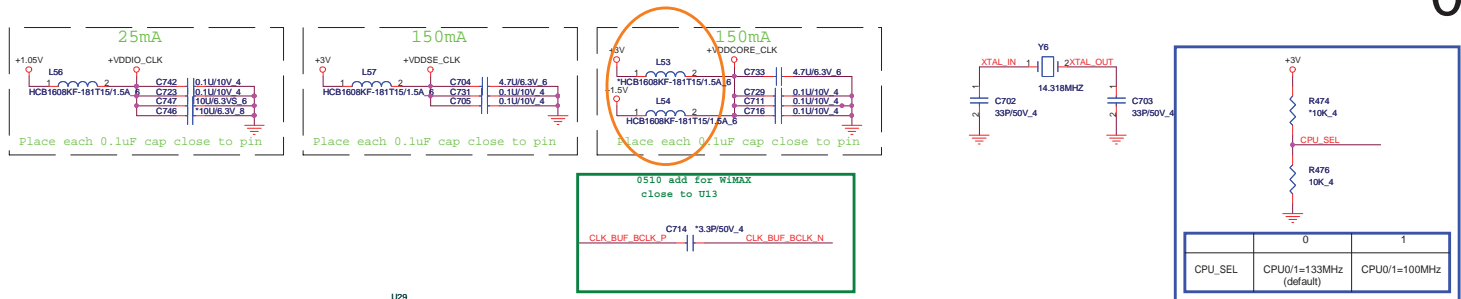


R18D INTEL UMA/DISCRETE SYSTEM DIAGRAM





+1.05V <10,11,12,14,41>

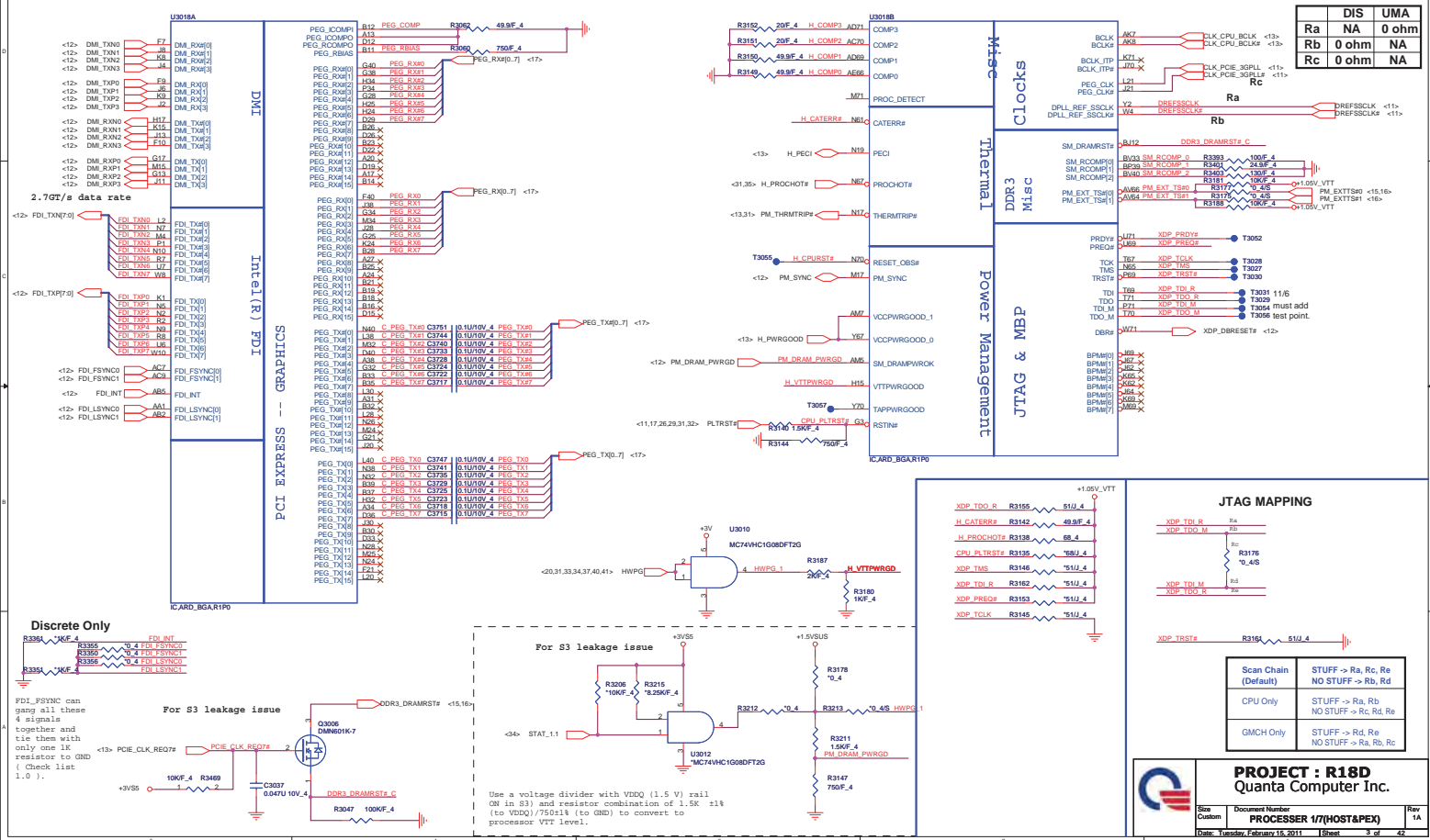
+1.5V <6,32>

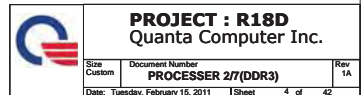
+3V <3,10,11,12,13,14,15,16,17,19,22,23,24,25,26,27,29,30,31,32,35,36,38>

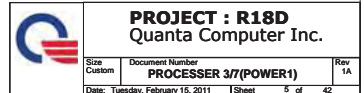


PROJECT : R18D
Quanta Computer Inc.

Size Custom	Document Number Clock Gen(9LRS3197)	Rev 1A
Date: Tuesday, February 15, 2011		Sheet 2 of 42

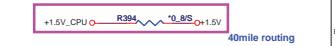
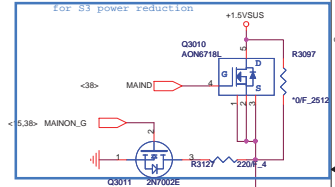
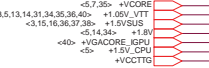
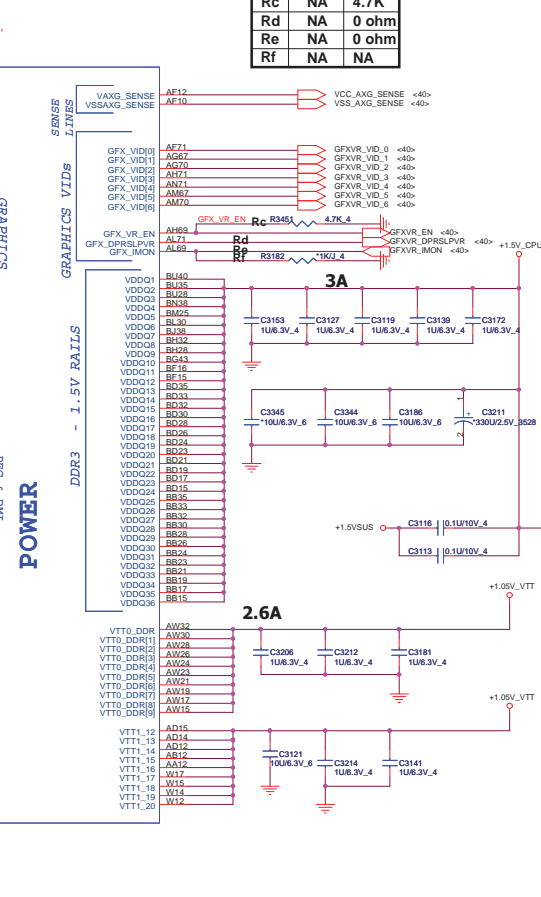
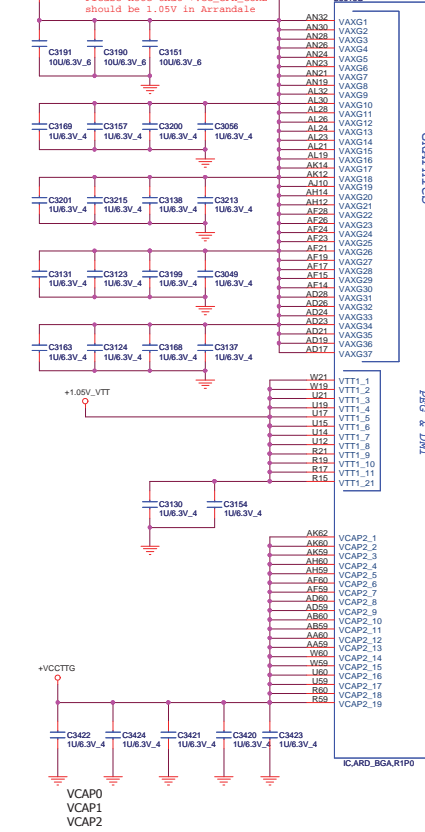






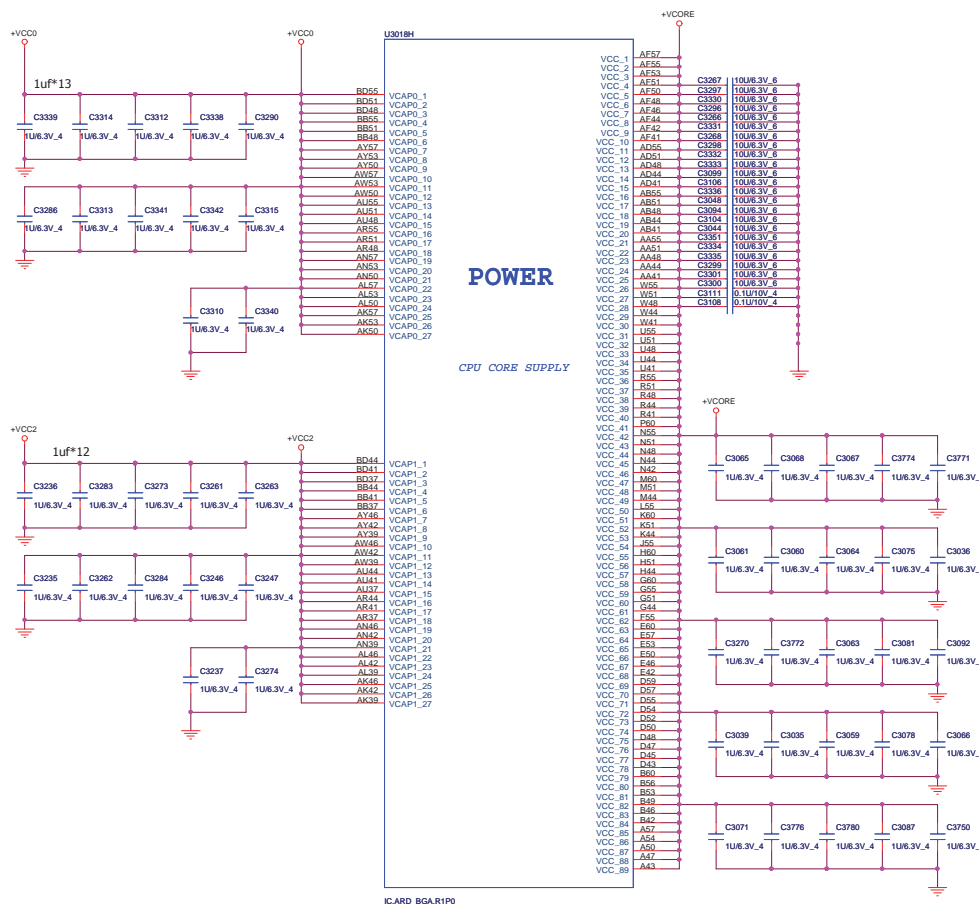
Max 22A VTT Rail Values are
Auburndal VTT=1.05V
Clarksfield VTT=1.1V


Please note that +VCC_GFX_CORE
should be 1.05V in Arrandale

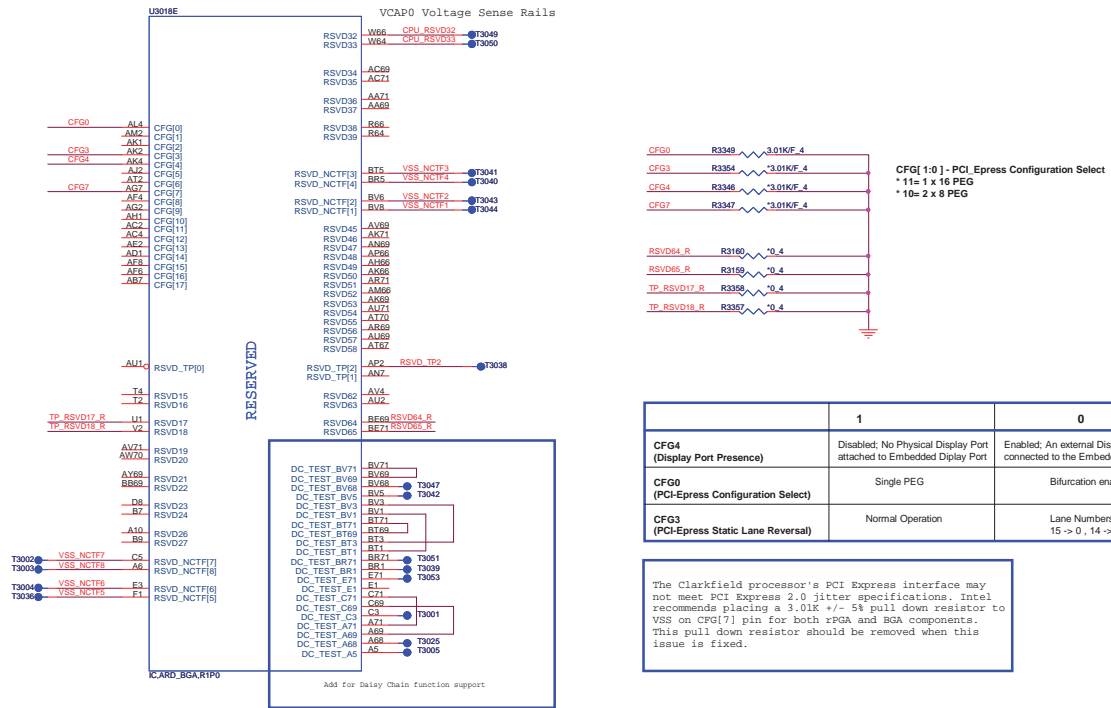


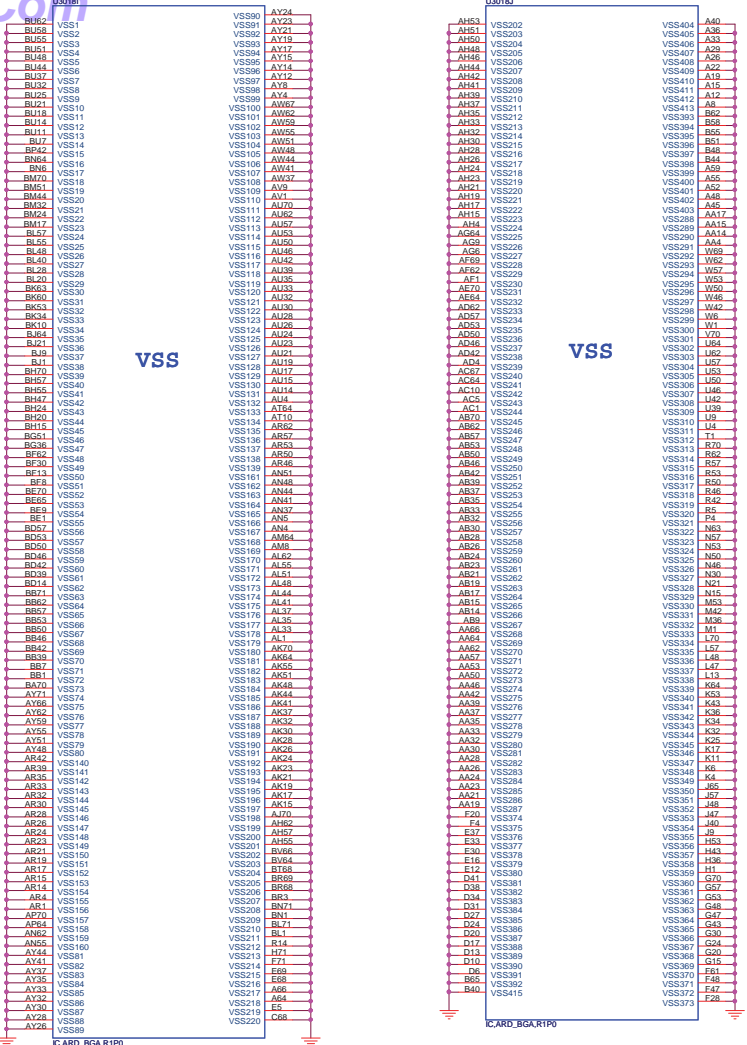
PROJECT : R18D
Quanta Computer Inc.


Size Custom	Document Number PROCESSOR 47(Power2)	Rev 1A
Date: Tuesday, February 15, 2011	Sheet	6 of 42



		
PROJECT : R18D Quanta Computer Inc.		
Size Custom	Document Number PROCESSER 57(POWER3)	Rev 1A
Date: Tuesday, February 15, 2011	Sheet	7 of 42



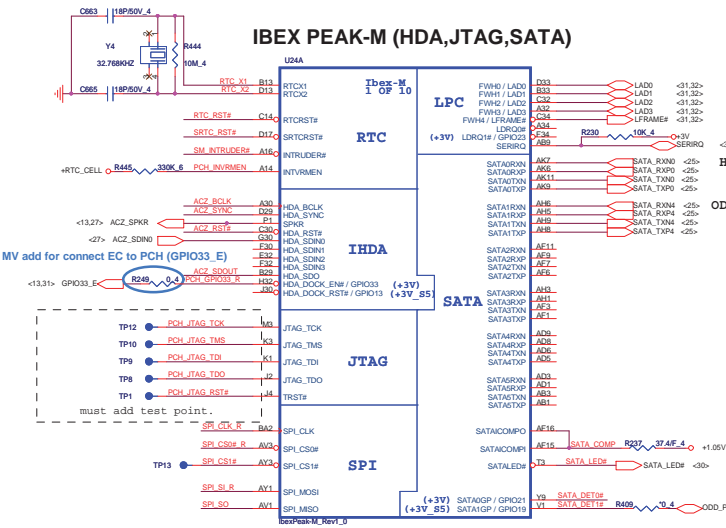




PROJECT : R18D
Quanta Computer Inc.

Size	Document Number	Rev
Custom	PROCESSOR 777(GND)	1A
Date: Thursday, January 13, 2011		Sheet 9 of 42

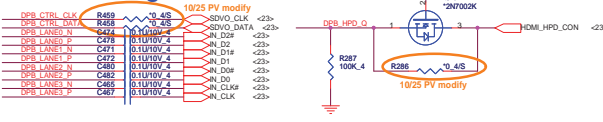
IBEX PEAK-M (HDA,JTAG,SATA)



1205 The SATALED# signal is
open-collector and requires a
weak external pull-up (8.2 k
to 10 k) to +V3.3.

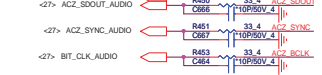


UMA HDMI signals



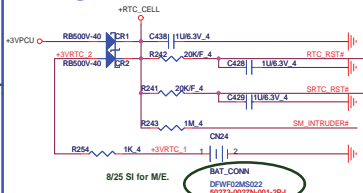
for AUDIO

<27> ACZ_RST#_AUDIO R452

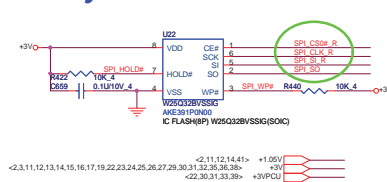


for MDC

RTC

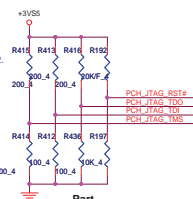
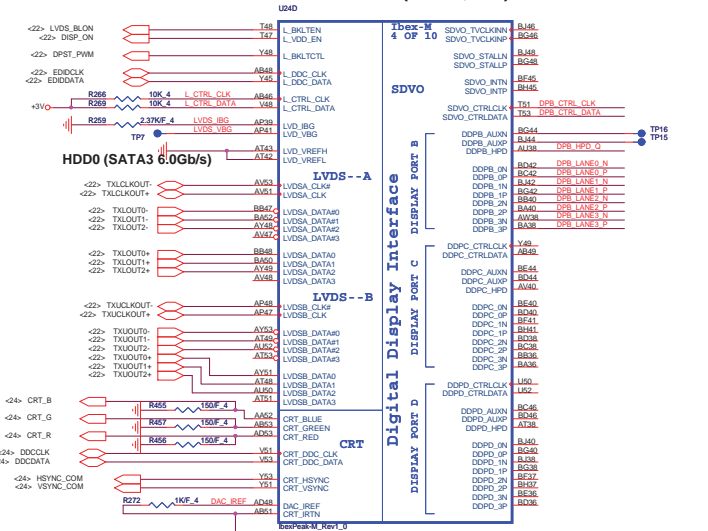


4M byte SPI ROM



UMA CRT,LVDS&HDMI signals

IBEX PEAK-M (LVDS,DDI)



For ES1 ONLY.NI for ES2

For ES1 ONLY.NI for ES2.

Part	Part Number	Part Description
------	-------------	------------------

Vender

Socket DG008000031

EON - EN25F32-100HIP

AKE39FN0Q00 IC FLASH(8P) EN25F32-100HIP (SOIC)

WINBOND - W25Q32BVSSIG

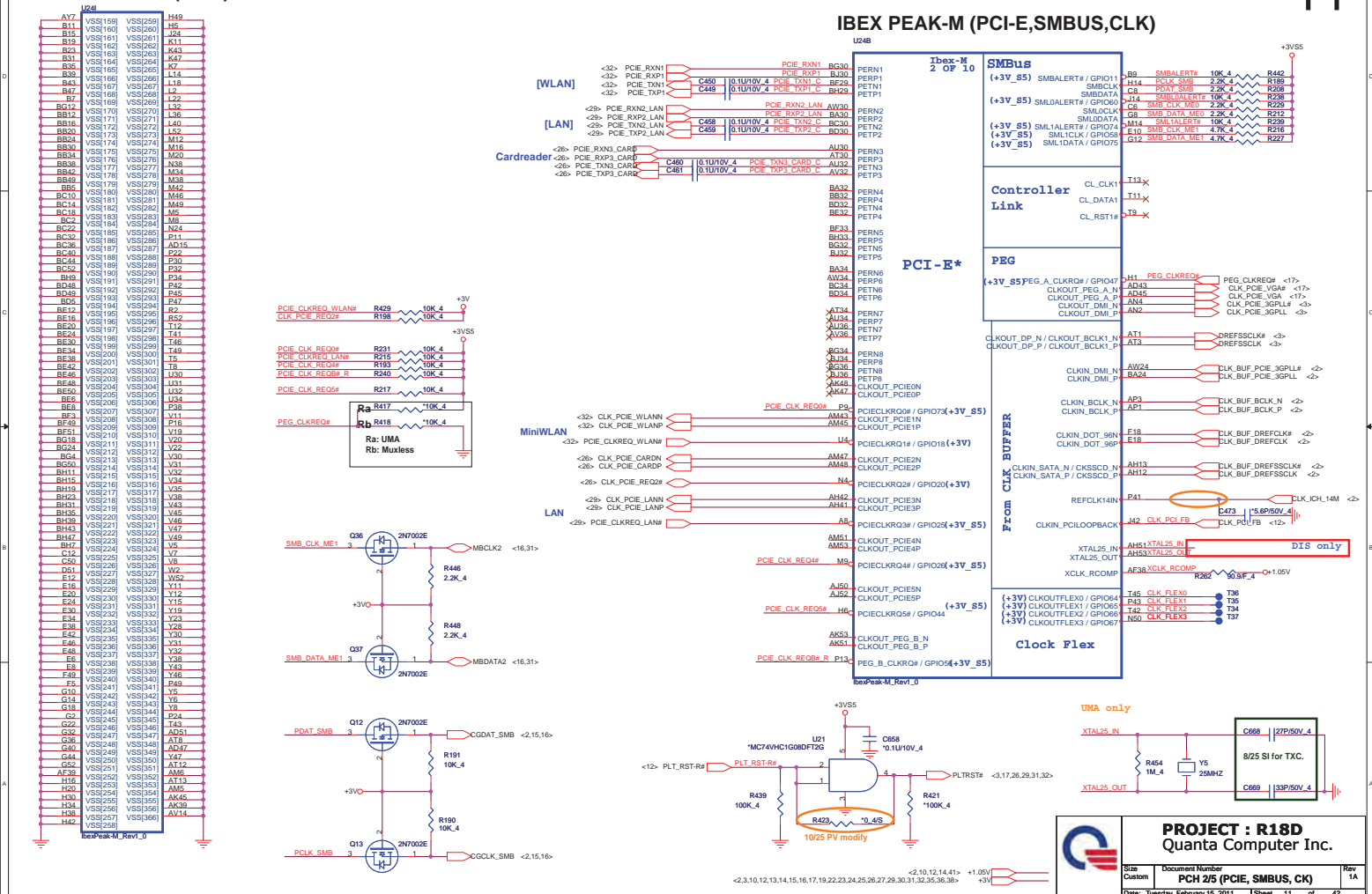


PROJECT : R18D
Quanta Computer Inc.

Size Custom	Document Number PCH 1/5 (SATA,HDA,LPC)	Rev 1.
Date: Tuesday, February 15, 2011 Sheet 10 of 42		

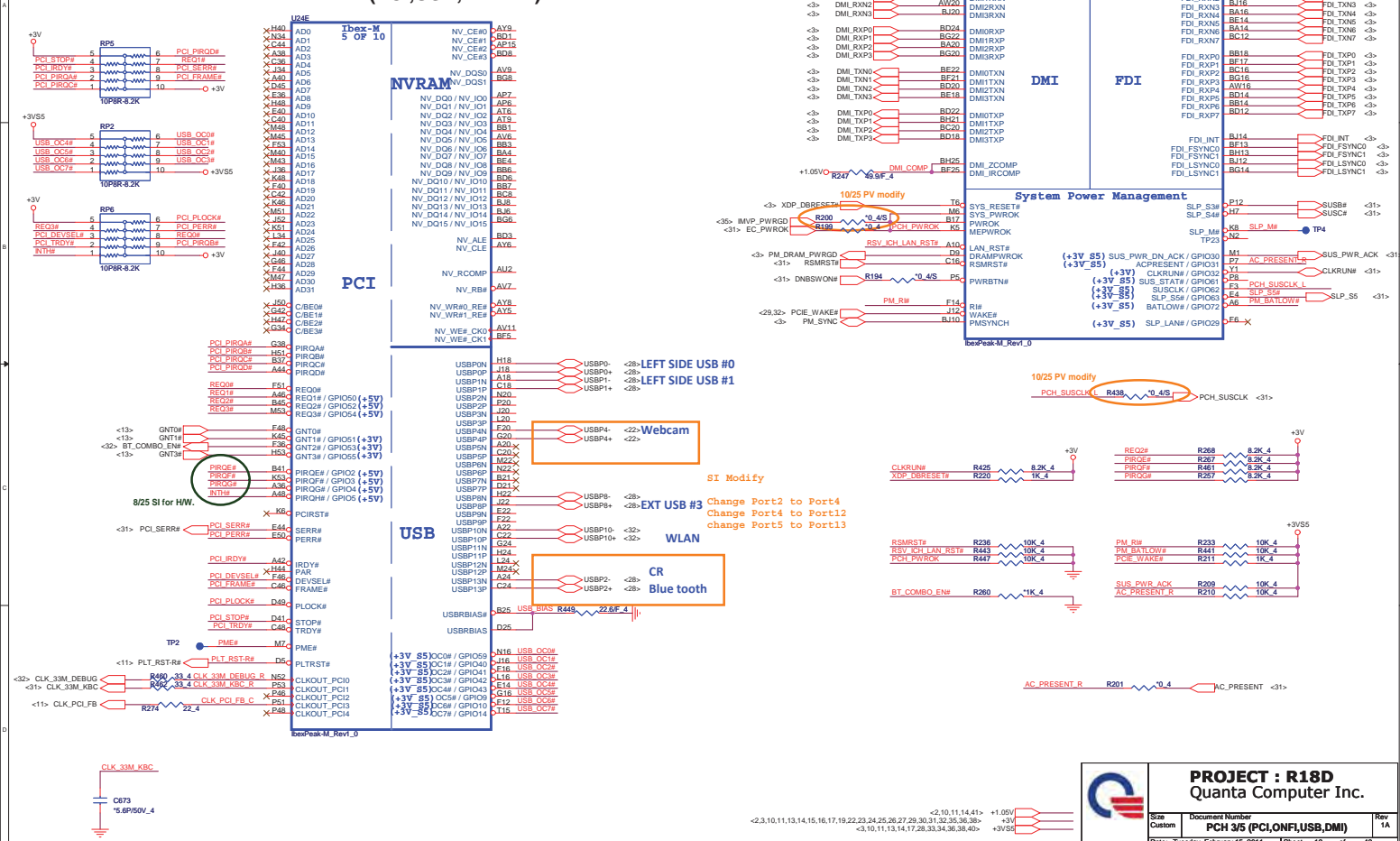
IBEX PEAK-M (GND)

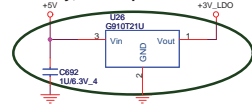
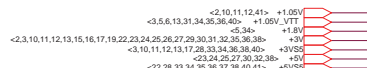
IBEX PEAK-M (PCI-E,SMBUS,CLK)



IBEX PEAK-M (DMI,FDI,GPIO)

IBEX PEAK-M (PCI,USB,NVRAM)

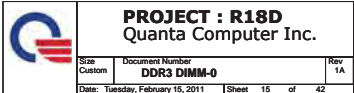


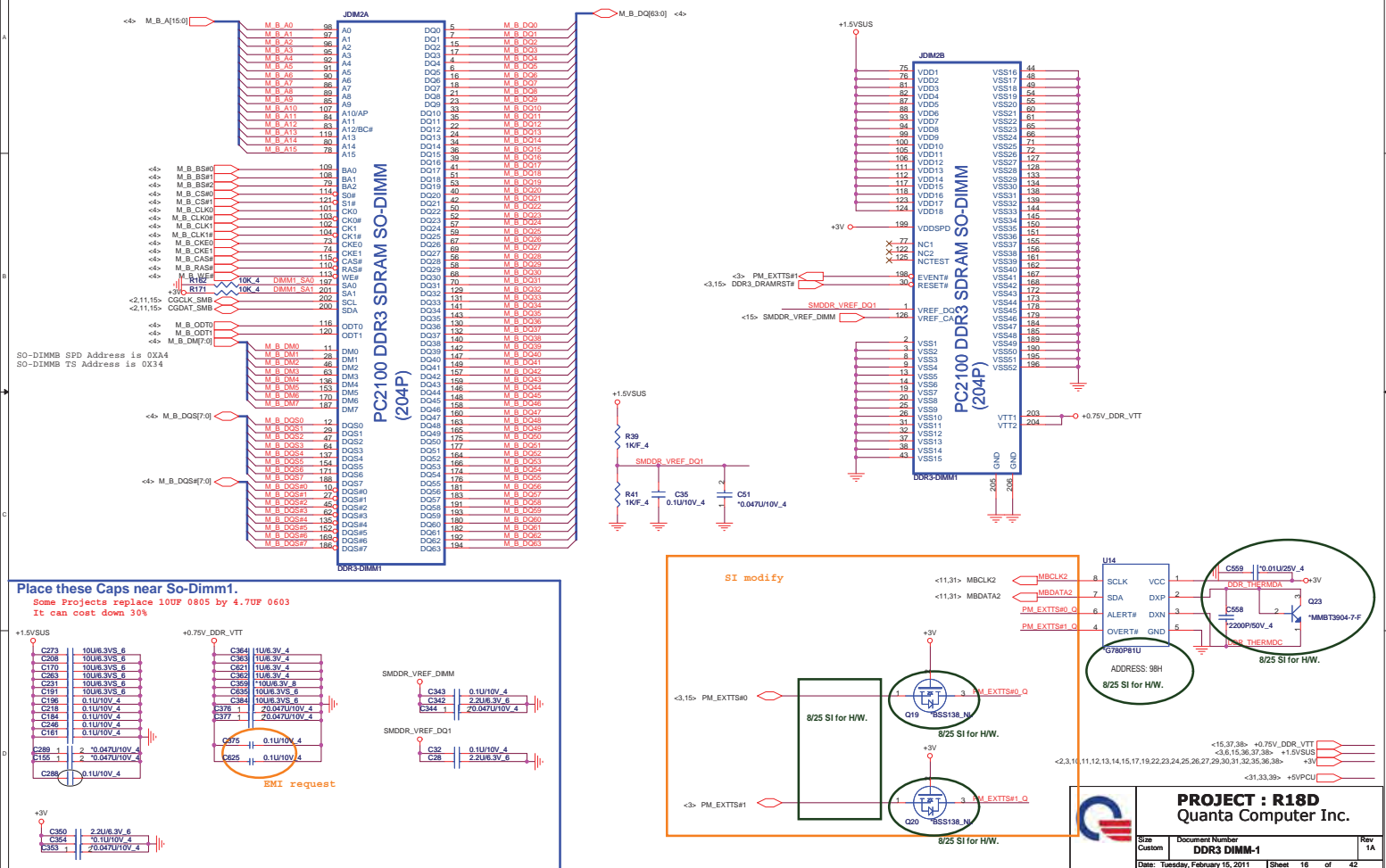


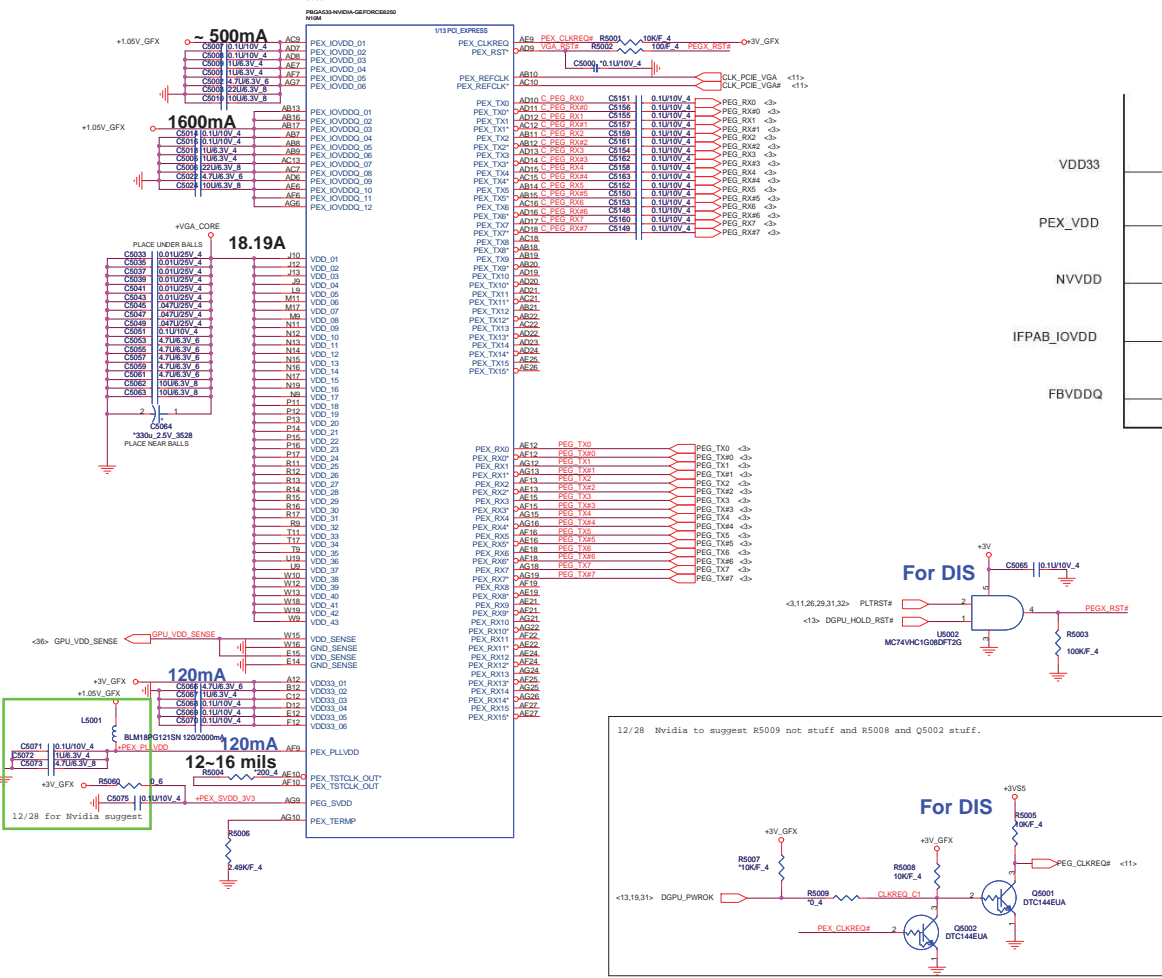
8/25 SI modify
Install LDO when UMA

	DIS	UMA
Ra	0 ohm	NA
Rb	NA	0 ohm
Rc	0 ohm	NA
Rd	NA	0 ohm

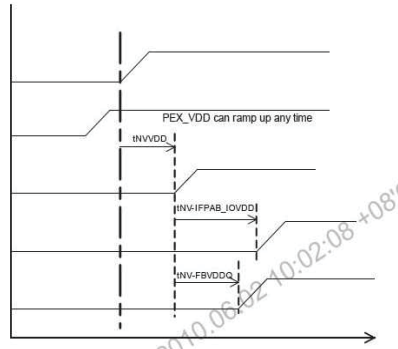
PROJECT : R18D Quanta Computer Inc.		
Size Custom	Document Number PCH 5/5 (POWER)	Rev 1A



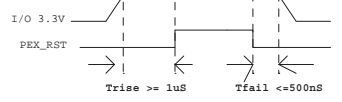




power up sequence

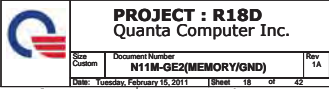


PEX_RST timing

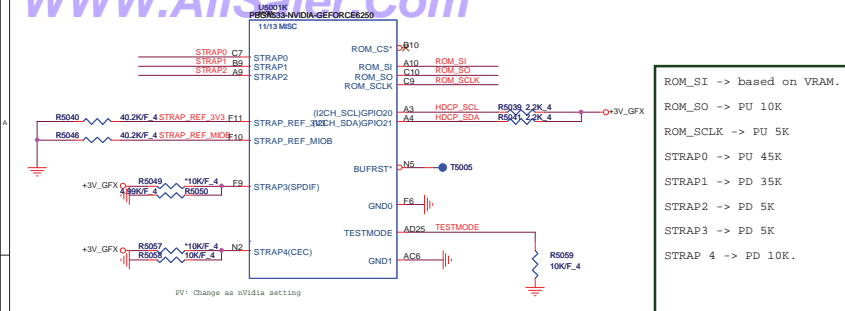


<3,10,11,12,13,14,15,16,18,22,23,24,25,26,27,29,30,31,32,35,36,38> +3V5S
 <18,20,36> +3V GFX
 <3> +1.05V GFX
 <3> +VGA CORE
 +3V

PROJECT : R18D		
Quanta Computer Inc.		
Rev	Document Number	Rev
1	N11M-GE2(PCIE/F)	1A
Date	Issued	Sheet
Tuesday, February 15, 2011	17	42

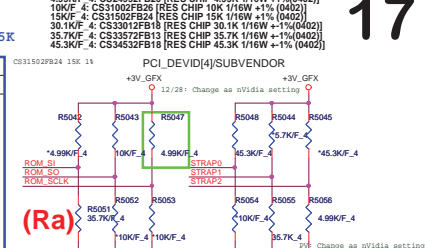






N12P-GV -> 0x17F
N12M-GE -> 0xA7A 1010 -> PU15K

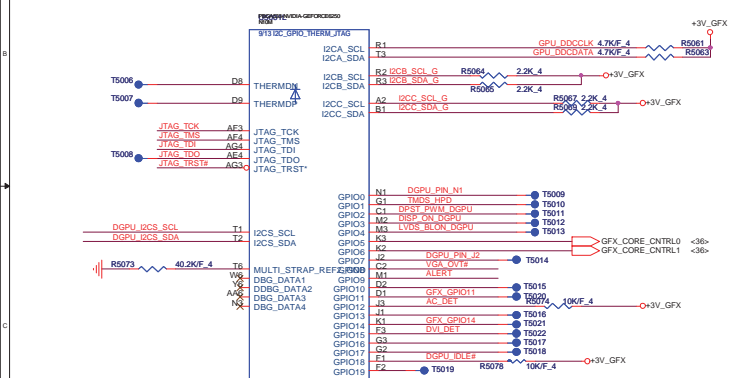
Logical Strap Bit Mapping		
	PU-VDD	PD
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111

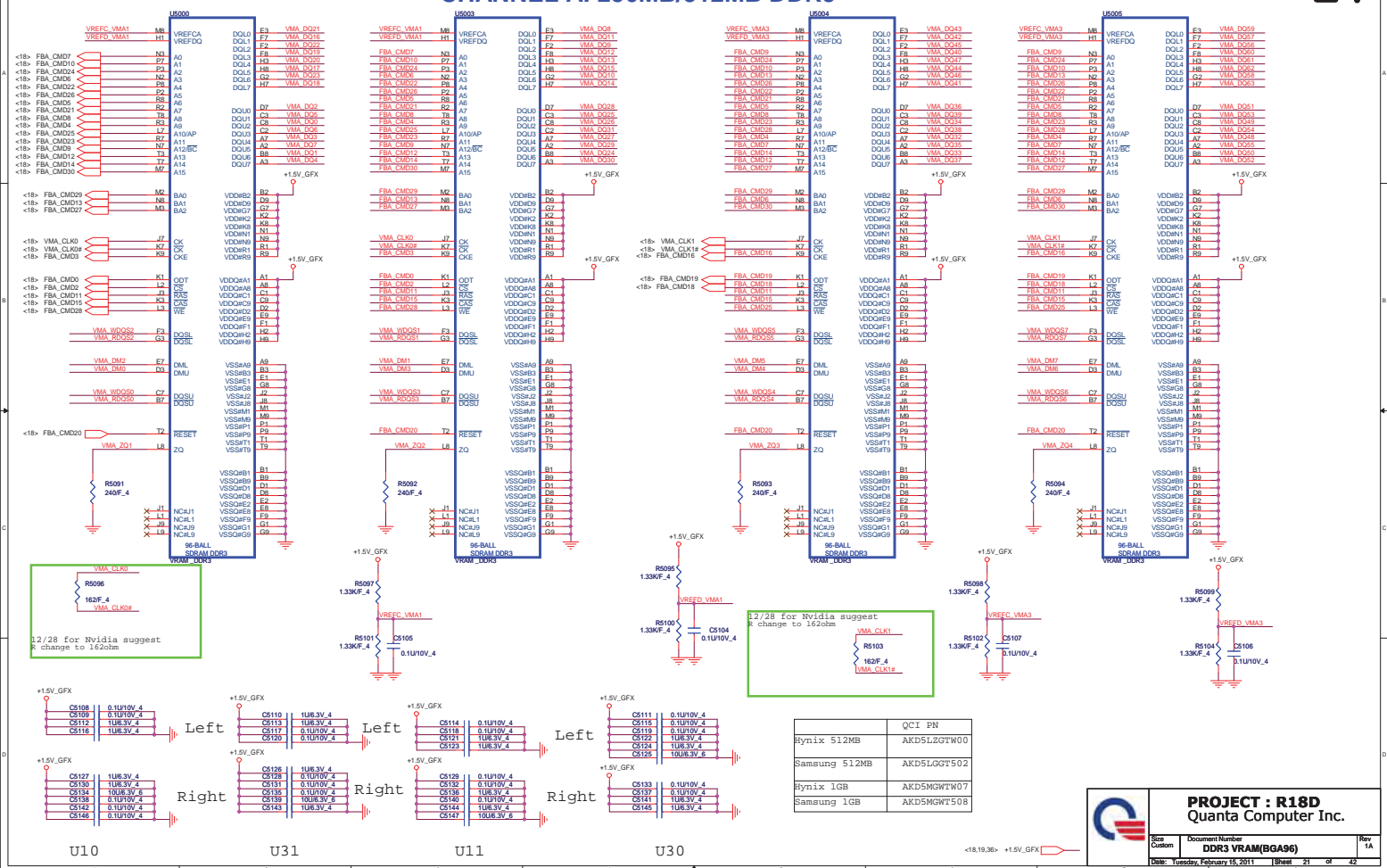


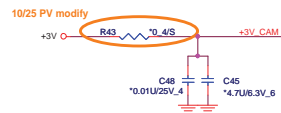
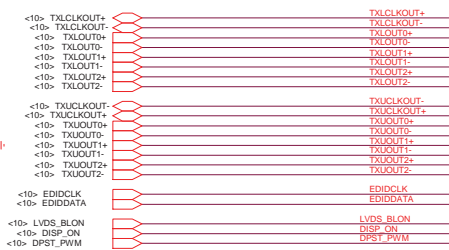
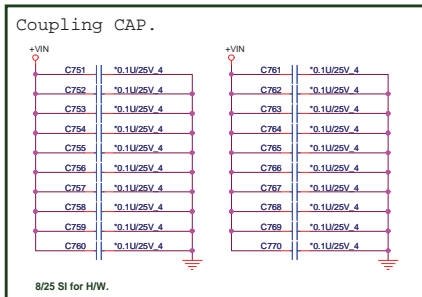
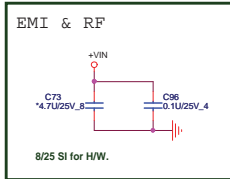
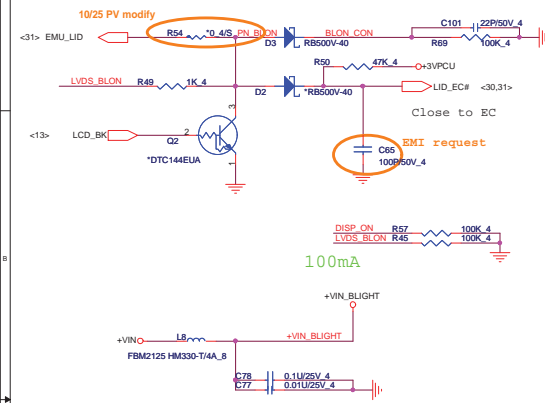
	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SO	XCLK_417	FB_0_BAR_SIZE	SMB_ALT_ADDR	VGA_DEVICE
ROM_SCLK	PCI_DEVID[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLL_EN_TERM
ROM_SI	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]
STRAP2	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
STRAP1	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]
STRAP0	USER[3]	USER[2]	USER[1]	USER[0]
STRAP3	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
STRAP4	RESERVED	RESERVED	PCIE_MAX_SPEED	DP_PLL_VDD33V

VRAM Configuration Table

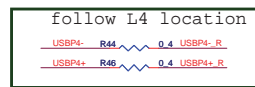
RAMCFG [3:0]	DESCRIPTION	Vendor	Vendor P/N	ROM_SI (Ra)
0000		Reserved		
0010	DDR3 64Mx16x8, 128bit, 1GB, 800MHz	Hynix		PD 15K
0011	DDR3 64Mx16x8, 128bit, 1GB, 800MHz	Samsung		PD 20K
0110	DDR3 128Mx16x4, 128bit, 1GB, 800MHz	Hynix		PD 35K
0111	DDR3 128Mx16x4, 128bit, 1GB, 800MHz	Samsung		PD 45K
XXXX				
XXXX				



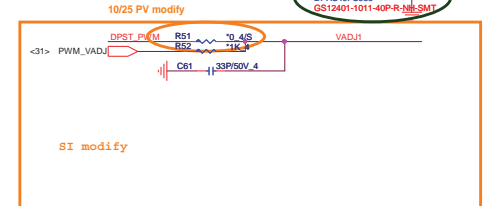
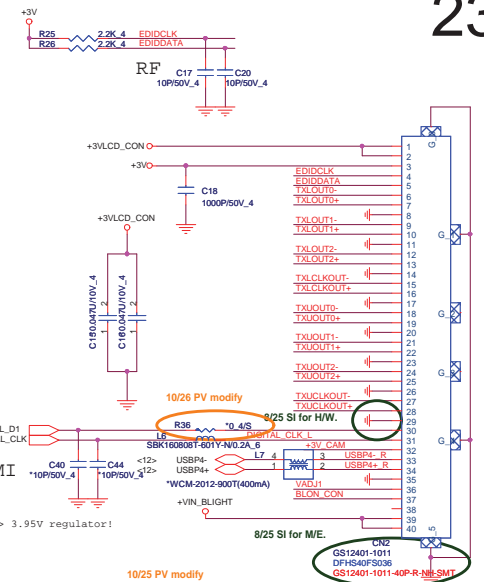
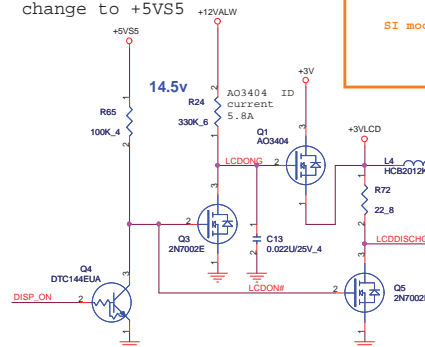





Please note that 2011 camera is +3V a We do not need to use 5V -> 3.95V regulator!



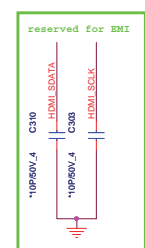
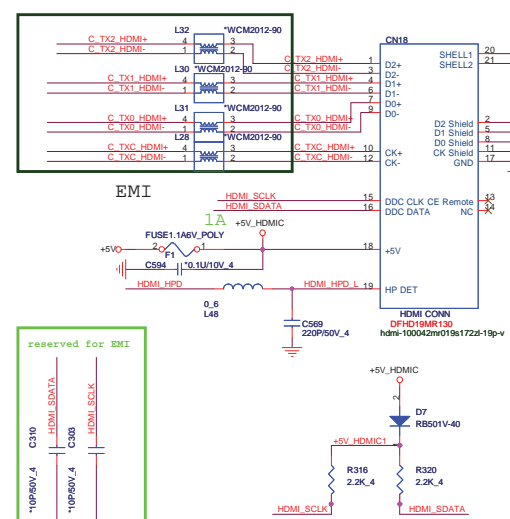
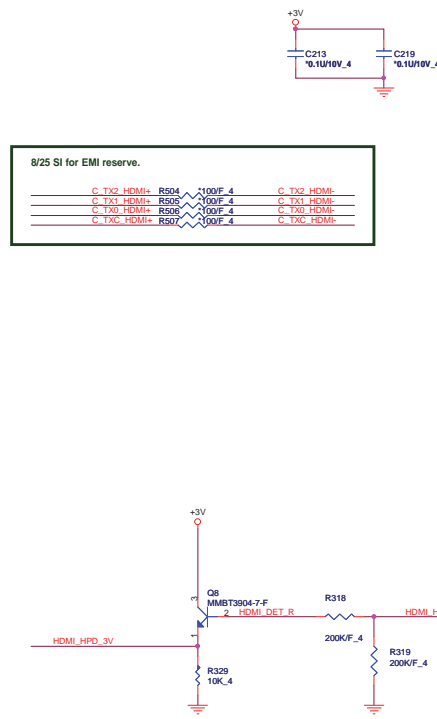
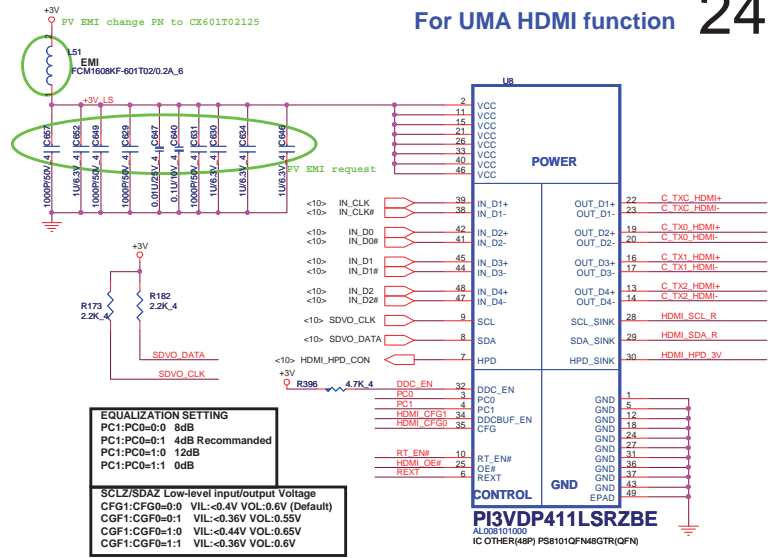
change to +5VS5 +12VALV



	PROJECT : R18D Quanta Computer Inc.		
	Size Custom	Document Number LCD CONN/LID/CAM	Rev 1A
Date: Tuesday, February 15, 2011		Sheet 22 of 42	

9/16 : PIM: need use ALP411LS000 or ALP411LS004 for capella

CHR : need Na R1182, add R1027 for capella



	PROJECT : R18D Quanta Computer Inc.		
	Size Custom	Document Number HDMI CONN	Rev 1A

Figure 1 displays the chemical structures of 15 ^1H -labeled nucleosides, arranged in two rows. The structures are labeled as follows:

- Top Row:**
 - H1: ^1H -c354d118p2
 - H8: O-R15D-1
 - H14: ^1H -c354d118p2
 - H11: ^1H -c354d118p2
 - H12: ^1H -C354d1158D118P2
 - H3: ^1H -c354d118p2
 - H8: ^1H -C354d1158D118P2
 - H4: ^1H -C354d1158D118P2
- Bottom Row:**
 - H2: ^1H -c236d118p2
 - H13: ^1H -tc354bc236d118p2
 - H15: ^1H -c354d118p2

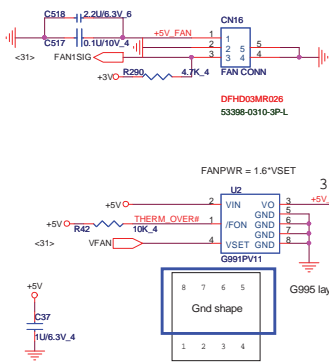
A box encloses the structures H13 and H15, with the text "8/25 SI for M/E." below it.



PROJECT : R18D
Quanta Computer Inc.

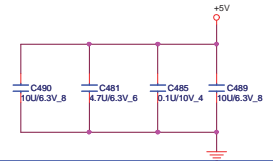
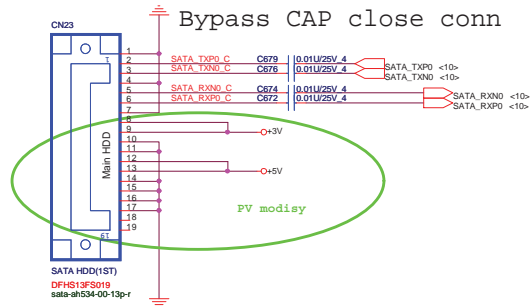
Size Custom	Document Number CRT,Hole	Rev 1A
Date: Tuesday, February 15, 2011	Sheet 24 of 42	

CPU FAN

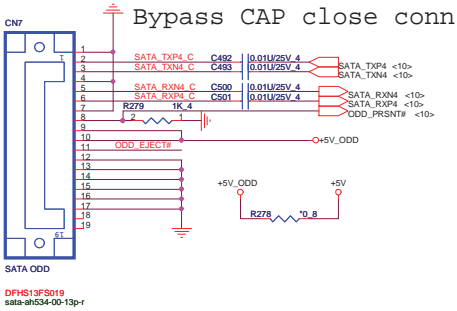


SATA HDD CONNECTOR

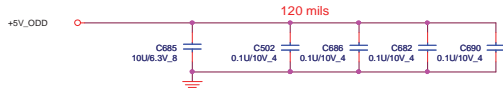
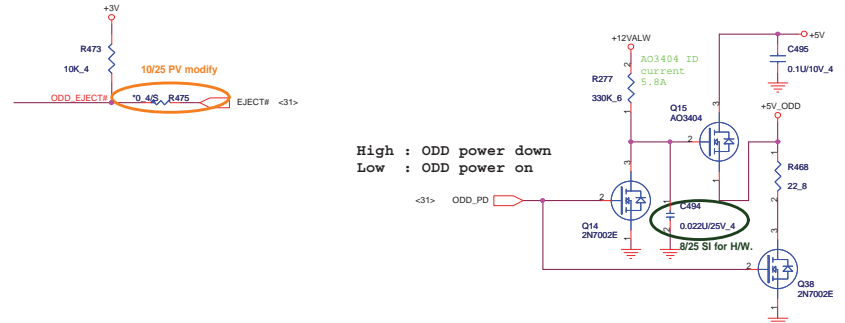
26



SATA ODD CONNECTOR

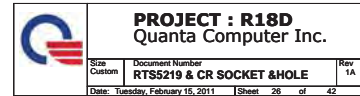


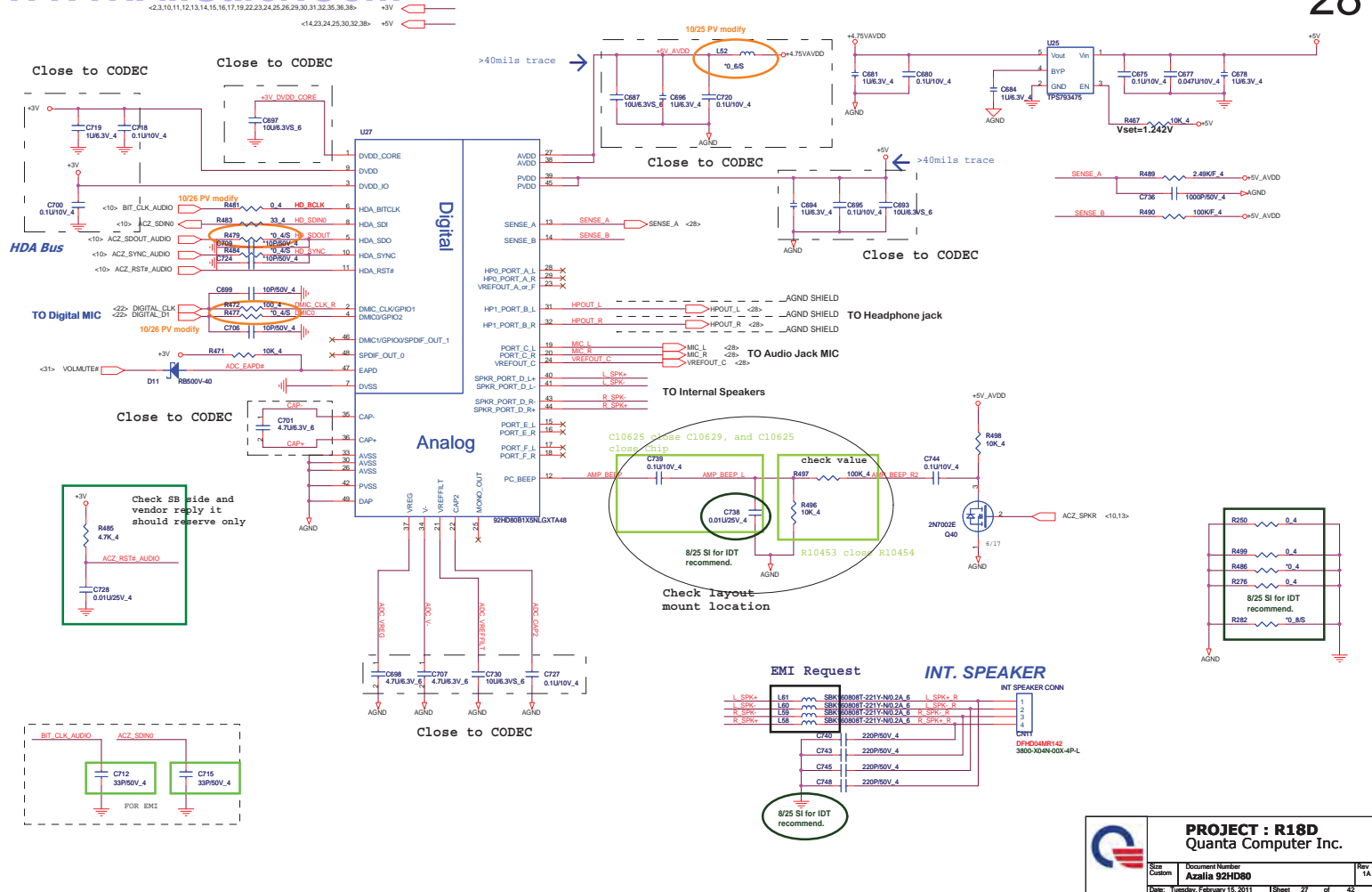
follow INTEL DG change eject PU to +3V.



PROJECT : R18D
Quanta Computer Inc.

Size Custom	Document Number HDD/ODD/FAN	Rev 1A
Date: Tuesday, February 15, 2011	Sheet 25 of 42	

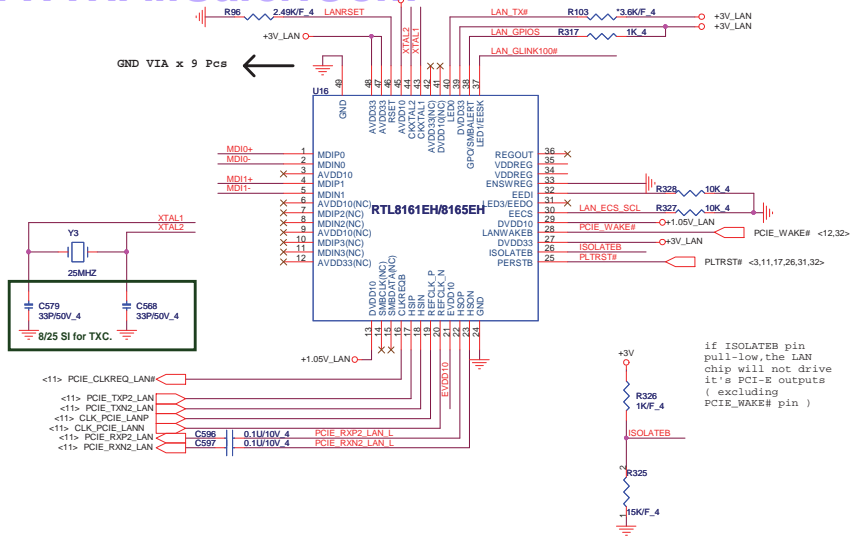




change to AL000547005

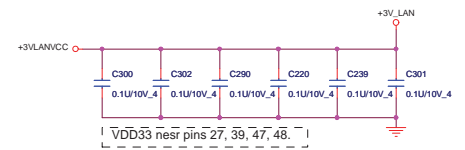
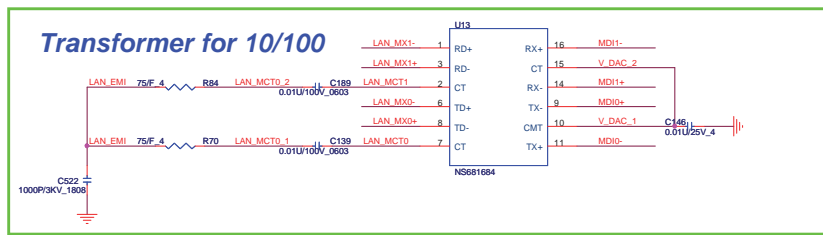
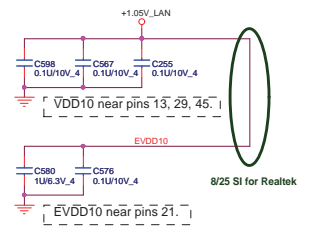


Size Custom	Document Number USB/BT/Audio Jack	Rev 1A
Date: Tuesday, February 15, 2011		Sheet 28 of 42

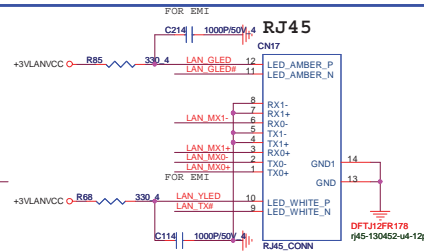
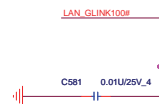
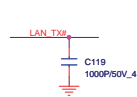


IND SMD 4.7UH +-20% 680MA (CBC2518T4R7M)
CV-4707MZ00

Power trace Layout 寬度> 60mil
>60mil



Lan Con.

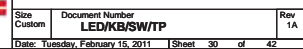


<2,3,10,11,12,13,14,15,16,17,19,22,23,24,25,26,27,30,31,32,35,36,38> <38> +3VLANVCC +3V

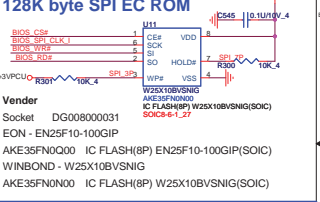
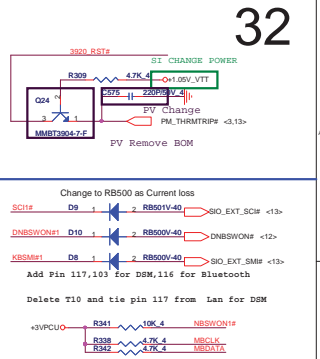
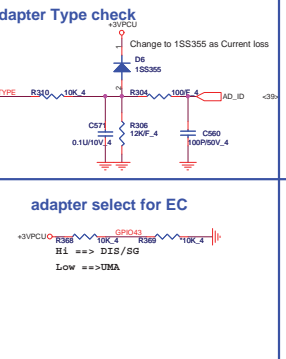
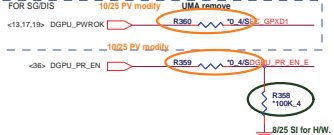
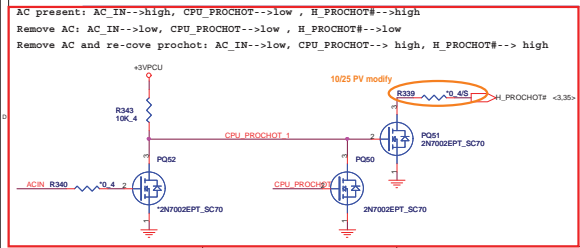


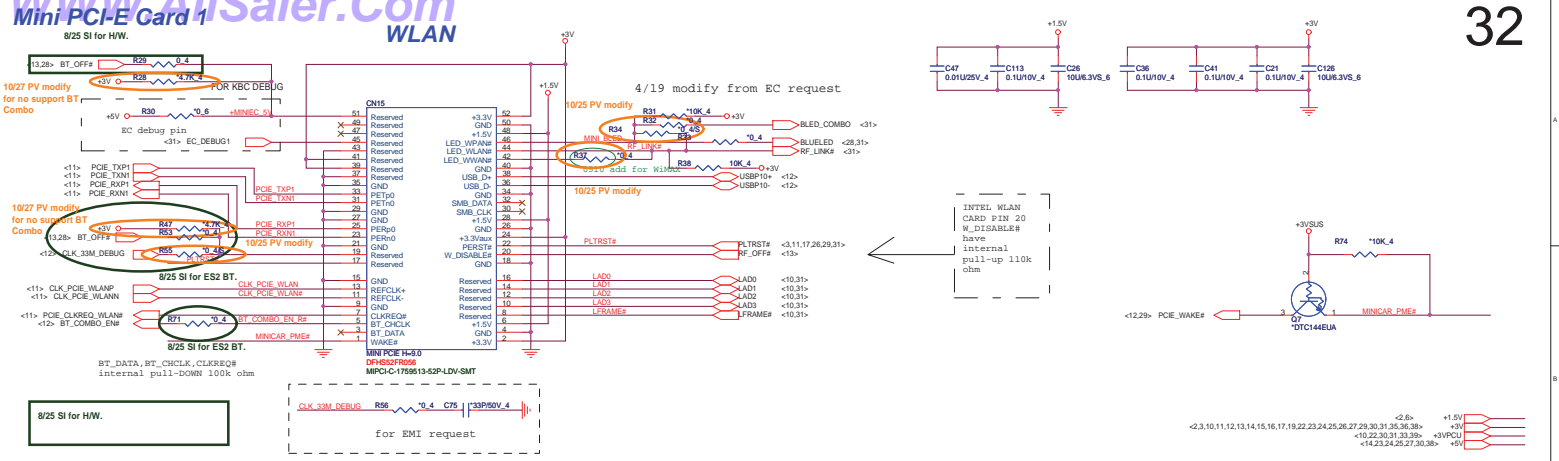
PROJECT : R18D
Quanta Computer Inc.

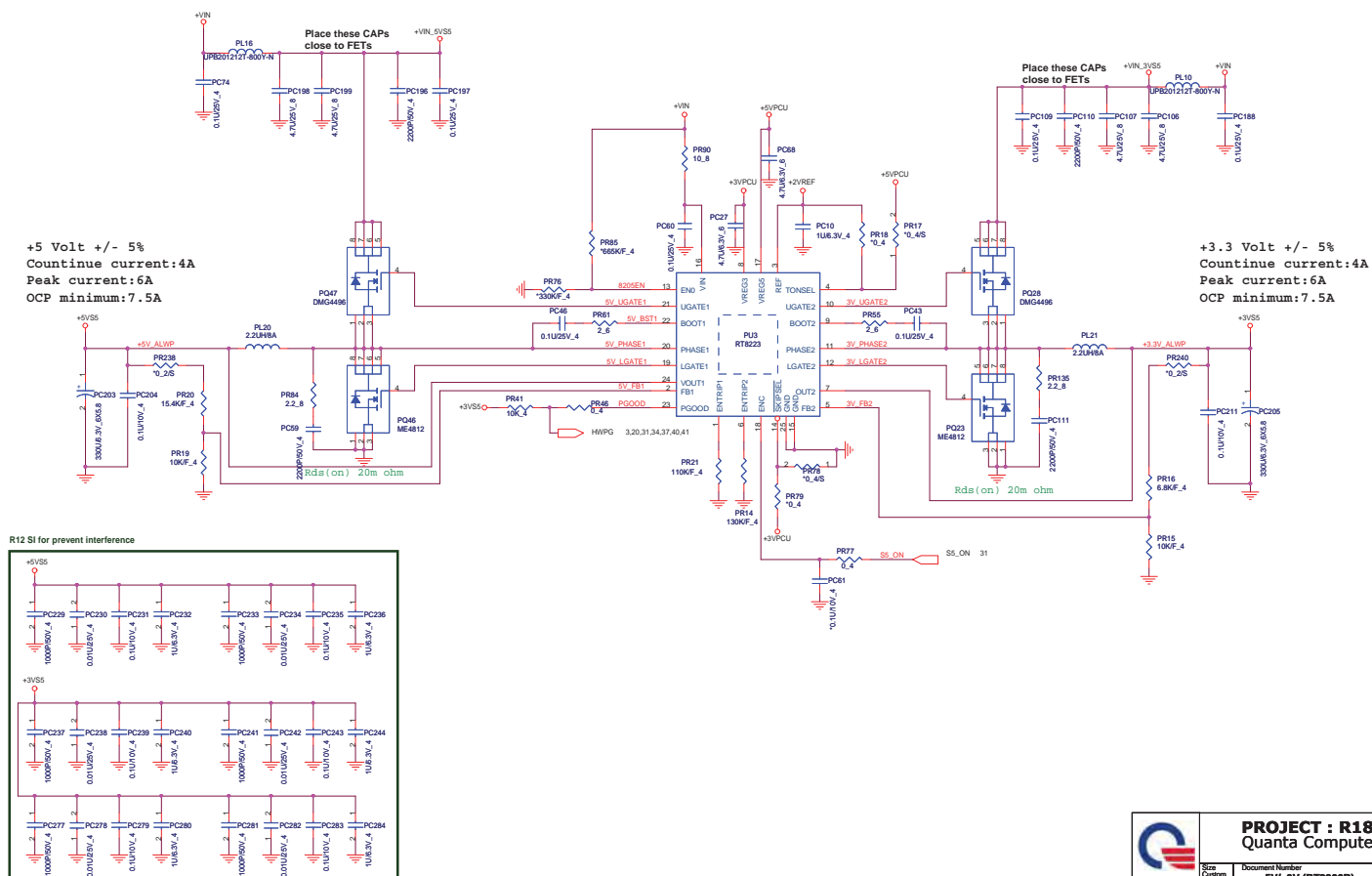
Size Custom	Document Number RTL8165EH	Rev 1A
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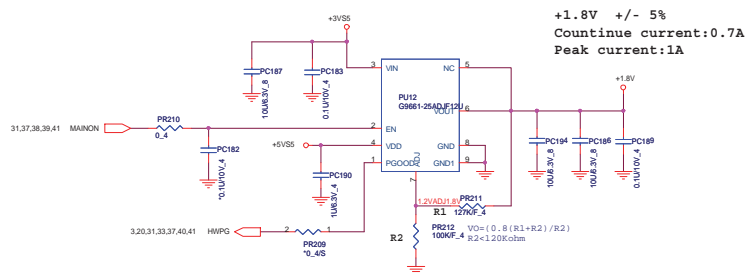
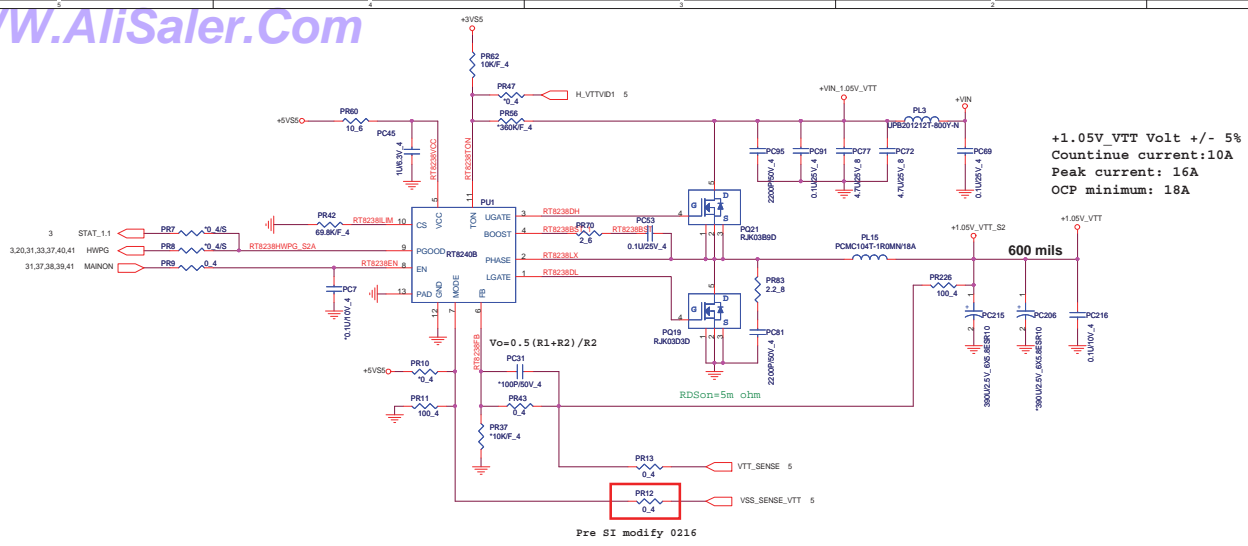


For GPU thermal



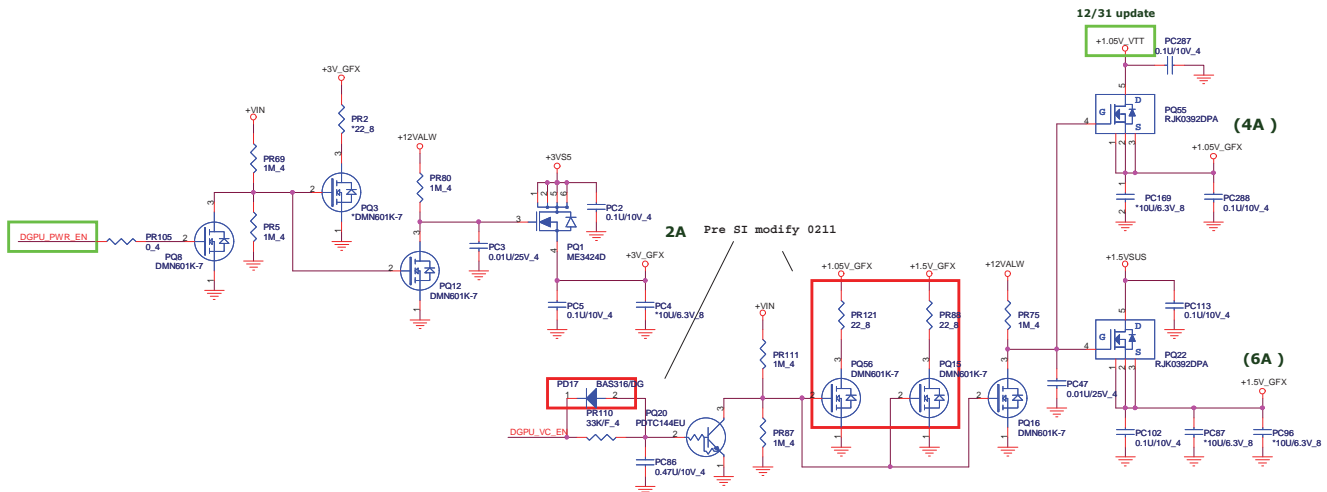
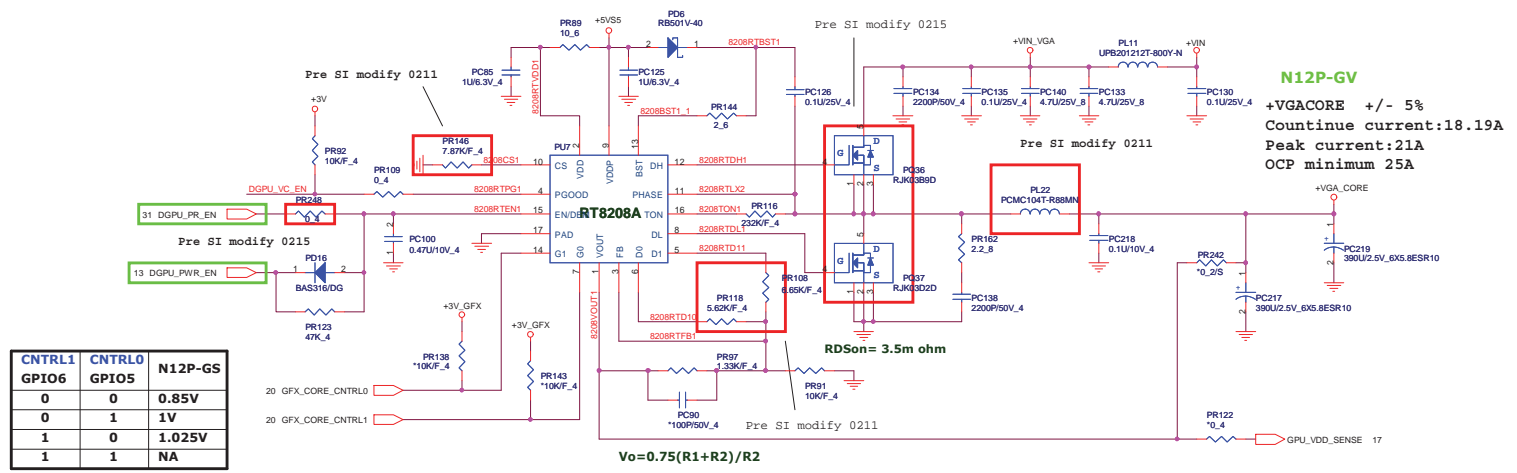





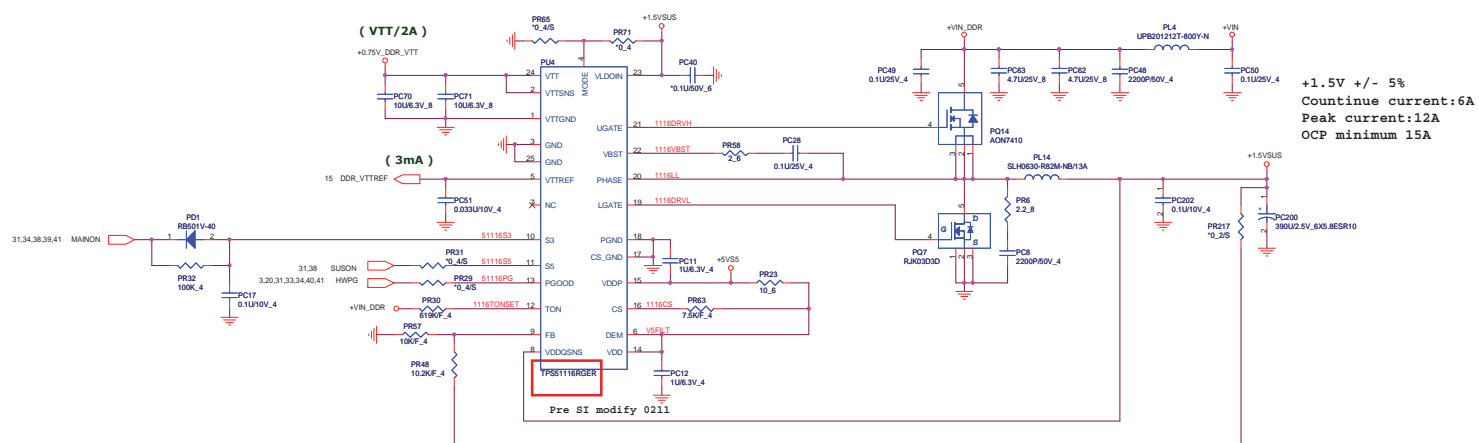



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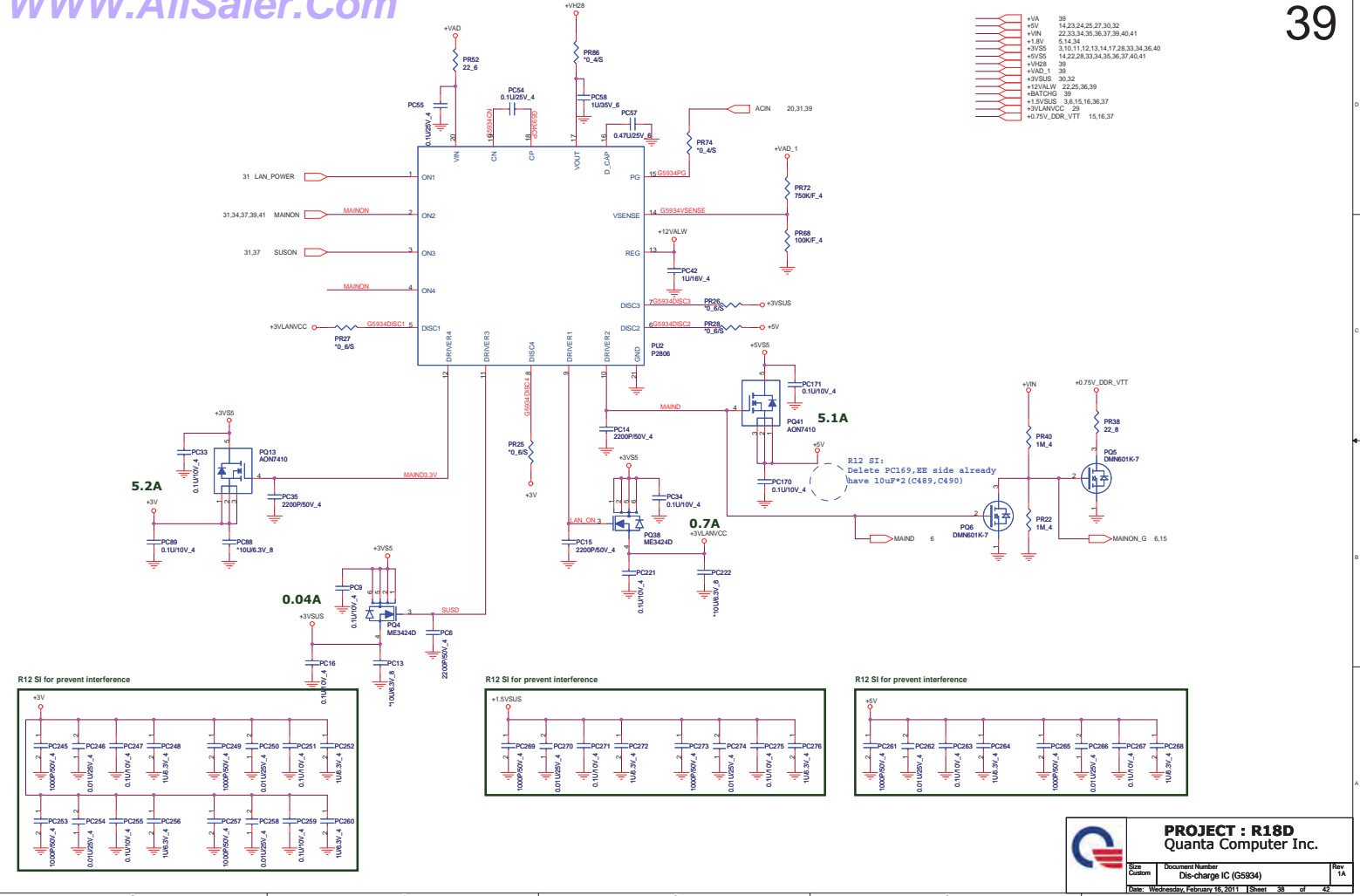


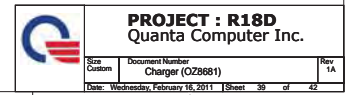


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-->Pre SI
Page 19
1.Delete L5005, C5096,C5097,C5098,C5099,C5100 and connect +SP_PLLVDD to +NV_PLLVDD
2.L5004 change to bead 220ohm (ESR=0.5) 0603.
3.C5085 change to 22uF_0805
Page 11
1.delete Q35.
Page 17
1.delete L5000 and C5074.
2.connect +3V_GFX to GPU ball A09 with a 0.1uF cap C5075.
3.New add R5060 for test
4.L5001 change to bead 120ohm@100MHz (ESR=0.18ohm) 0603.
5.C5073 should be 4.7uF_X7R_0805.
6.C5072 should be 1uF_X7R_0603.
7.C5071 should be 0.1uF_X7R_0402.
8.PCIE change to PEX_TX0-7 and PEX_RX0-7 on GPU side for X8 lane configuration
9.unstuff R5009 and R5008 Q5002 stuff for test
9.delete L5002 for Widi recommend
Page 18
1.L5003 change to bead 30ohm (ESR=0.01) 0603.
2.C5085 change to 1uF_X7R_0603
3.Delete C5084.
Page 21
1.R5096 and R5103 change to 162ohm_1%.
Page 31
1.New add R5105 and R5106 2.2K pull up resistors to +3V for GPUT_CLK and GPUT_DATA on EC side.
2.Delete D20,Q25,D19,R500.
Page 20
1.delete R5081,R5082,R5082.
2.New add R5085 and R5086 10K pull down resistors to GFX_CORE_CNTRL0 and GFX_CORE_CNTRL1
3.Change R5047 to 5K pull up for ROM_SCLK
4.Change R5080 to 10K for JTAG_TRST# pull down.
5.R5084 can be no stuff for JTAG_TCK
6.New add Q5010 for AC/Batt# function.
7.New add Q5011.



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Quanta Computer Inc.

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